Full-power converter based test bench for low voltage ride-through testing of wind power converters

International Conference E/E Systems for Wind Turbines Dr. Riku Pöllänen, The Switch 11.5.2011



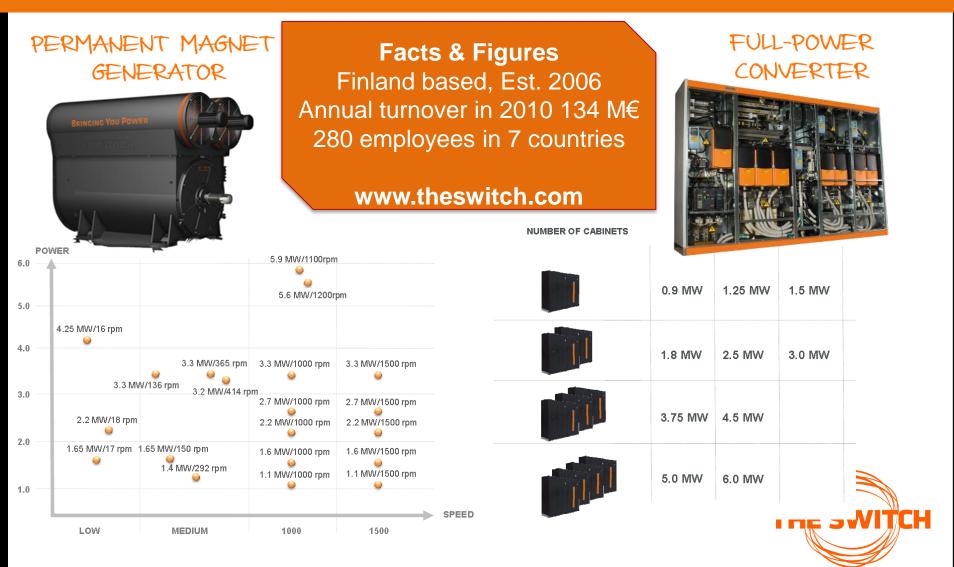
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 - Grid Code FRT requirements
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The Switch introduction



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Grid codes

- Grid codes are national minimum technical regulations and requirements for interconnection that an electrical generating unit must fulfill
- O Purpose of the grid codes is to secure a reliable, safe and efficient operation, maintenance and functioning of the electrical grid
- The main requirements common to most of the grid codes:
 - Voltage and frequency operating range
 - Active power control / Frequency control
 - Reactive power control / Voltage control
 - Sault Ride Through (FRT)
 - Low-Voltage Ride-Through (LVRT)
 - O High-Voltage Ride-Through (HVRT)



Grid code FRT requirements

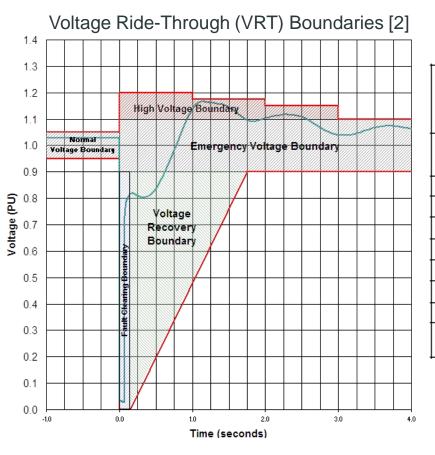


Table 1: Summ ary of national fault ride-through requirements - source [1].

		Faultride-fbrough capability					
Condity	Voltage Level	Fault duration	Voltage drop level	Recovery time	Voltage profile	Reactive Current injection	
Dennank	DS	100 m sec	25%Ų	læc	2,3-ph	no	
	TS	100 m sec	25%Ų	læc	1, 2, 3-ph	no	
Ire h nd	DS/TS	625m sec	15%U,	3 se c	1,2,3-ph	no	
Gemany	DS/TS	150m sec	0%U,	1.5 sec	Generic	Up to 100%	
Gneat Britain	DS/TS	140m sec	15%Ų	12sec	generic	no	
Spain	TS	500m sec	20%U,	læc	generic	Up to 100%	
Italy	>35kV	500m sec	20%U,	03sec	generic	no	
USA	TS	625m.sec	15%.U,	23sec	generic	no	
Ontario	TS	625m sec	15%Ur	-	-	no	
Quebec	TS	150m sec	0%U,	0.18sec	Positive se quence	no	

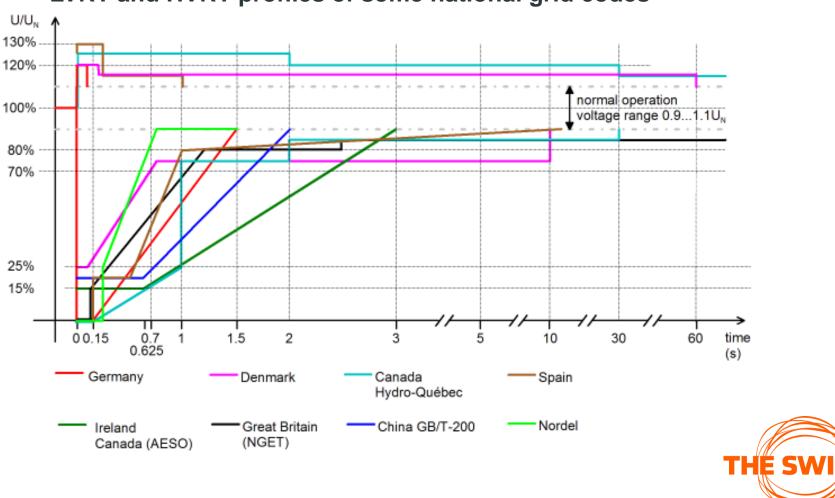
[1] F. lov et al., *Mapping of grid faults and grid codes*, Risø-R-1617(EN), Risø National Laboratory, July 2007

[2] The Technical Basis for the New WECC Voltage Ride-Though (VRT) Standard, June 13 2007, Available: http://www.wecc.biz/Standards/Development/



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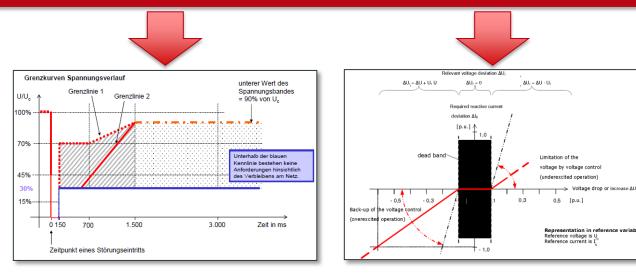
Grid code FRT requirements



LVRT and HVRT profiles of some national grid codes

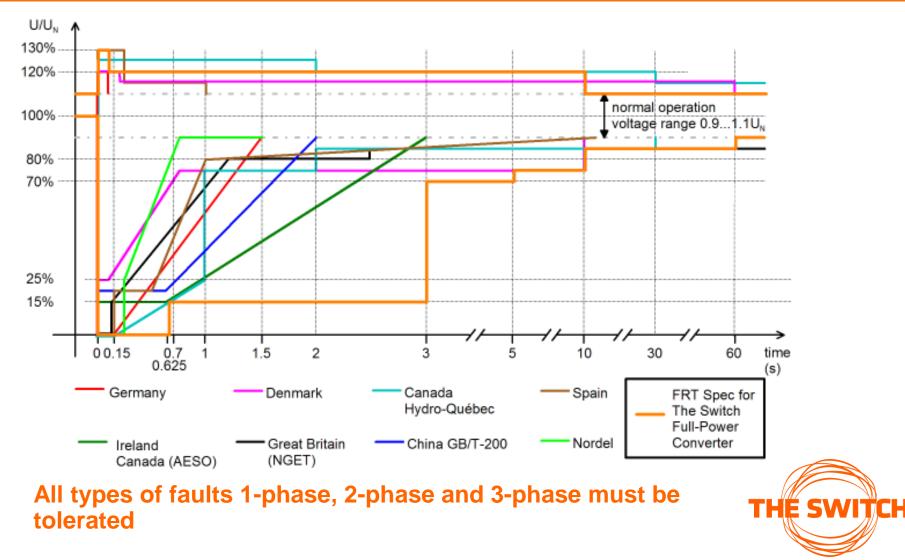
Grid code FRT requirements

- 1. Stay connected during the grid faults (VRT boundaries)
- 2. Fast active power restoration to pre-fault values
- 3. Support network voltages during a fault with reactive current (optional)
- 4. Distribute short circuit current during a fault (optional)





FRT control development of The Switch Full-Power Converters



FRT control development of The Switch Full-Power Converters

- Improved grid converter control to meet the latest FRT requirements
 - OZero or very low voltage level (Ugrid < 15% Un) duration up to 625 ms</p>
 - Improved persistence of grid synchronism during low grid voltage levels and voltage restoration
 - Fault type detection

Improved FRT performance and fault type detection is based on

- Seedforward control from measured grid voltage
- O Intelligent "flywheel logic" to keep the synchronism during low voltage levels
- O Extraction of symmetrical components of grid

Some inbuild FRT functionalities

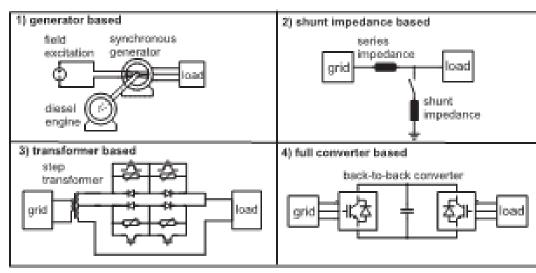
- O Extraction of symmetrical components of grid voltage
- O Reactive current injection during LVRT, ZVRT and HVRT
- Selection of operation mode during FRT



LVRT testing of wind power converter

O Generally four types of voltage dip generator systems:

- 1. Rotating generator based
- 2. Shunt (or switched) impedance based
- 3. Transformer based
- 4. Full-power converter based
- Shunt impedance based solutions
 - Most often used
 - Recognized as a standardized (de facto) way to create voltage dips



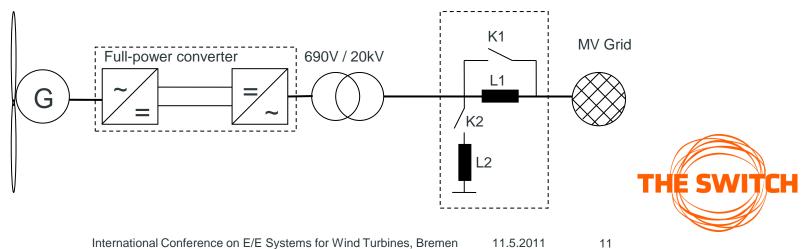
C. Wessels et al., Transformer Based Voltage Sag Generator to perform LVRT and HVRT Tests in the Laboratory, *In Proceedings of EPE-PEMC 2010*, Ohrid, Republic of Macedonia.

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Shunt impedance based FRT test system

- Challenges for R&D testing at the manufacturing site
 - Full-power grid connection and sufficiently high SCR needed
 - O Upstream grid disturbance
 - O Bulky circuit breakers and reactors needed
 - O Mobile test container solutions are expensive
 - Setup time for different test cases
 - In practice, a limited number of voltage dip types can be generated
 - Special requirement for installation and operation in case of MV level system



Full-power converter based LVRT test bench

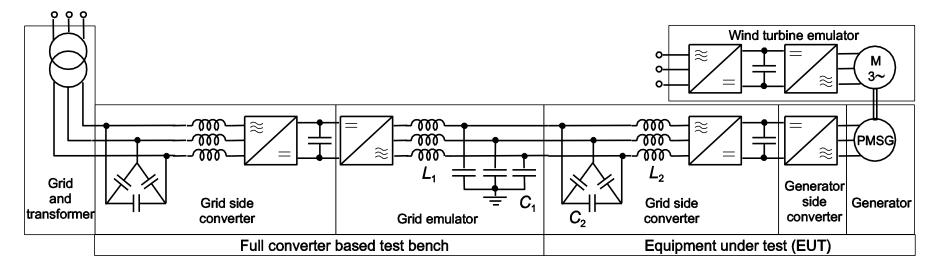


Table: Main parameters of full-converter test benches

Parameter	Down-scaled	Full-scale	
Line voltage U_n [V]	400	690	
Power S _n [kVA]	8.2	1800	
Filter inductance L_1 [mH]	1.7	0.05	
Filter capacitance C_1 [µF]	1	68	
Filter inductance <i>L</i> ₂ [mH]	4.1	0.09	
Filter capacitance C_2 [µF]	2.2	204	
Max DC-link voltage U_{dc} [V]	750	1100	
Switching frequency f_{sw} [kHz]	3.6	3.6	

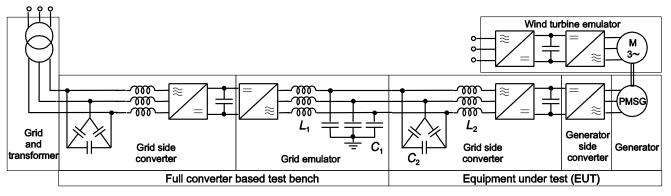


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Full-power converter based LVRT test bench

Seatures

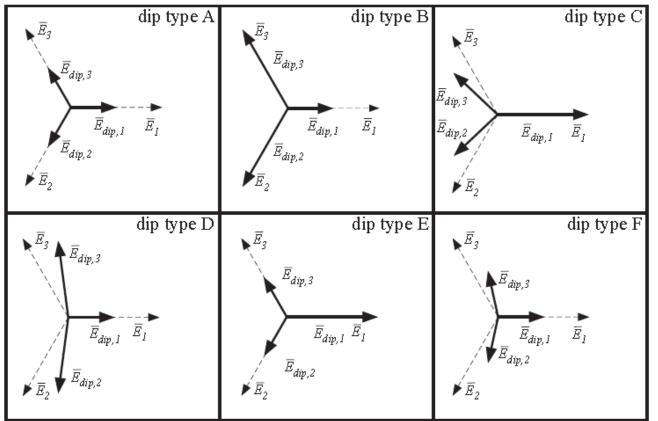
- Only partial-power grid connection needed
- Negligible upstream grid disturbance
- Second Second
- Seasy and fast setup of different test cases
- Various types of voltage dips can be generated
- Arbitrary dip depth (fault factor k), duration and number of consecutive dips can be generated
- HVRT, phase jumps, frequency ramps also possible
- O No moving parts in the dip generation system





Voltage dip classification

Phasors of three-phase voltages before (dashed) and during the fault (solid)



M. Bongiorno, On Control of Grid-connected Voltage Source Converters – Mitigation of Voltage Dips and Subsynchronous Resonances, Dissertation, Chalmers University of Technology, Gothenburg, Sweden, 2007.



Voltage dip propagation and generation

Fault	Dip in HV level	Dip in MV level	Dip in LV level	Generation (LV)
3-phase fault	Туре А	Туре А	Туре А	u' = (1 - k)u $v' = (1 - k)v$ $w' = (1 - k)w$
1-phase fault	Туре В	Туре С	Туре D	u' = (1 - k)u $v' = v + k u/2$ $w' = w + k u/2$
phase-to- phase	Туре С	Type D	Туре С	u' = u v' = v - k(v - w)/2 w' = w + k(v - w)/2
2-phase to ground	Туре Е	Туре F Туре Е	Type G (C) Type F	u' = (1 - k)u v' = v + k(u - v)/3 w' = w + k(u - w)/3

Coefficient k = 0...1 is the fault level factor.

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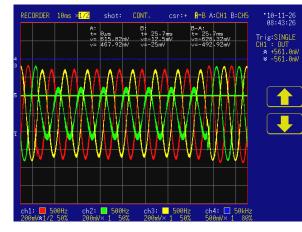
Voltage dip generation - Examples

csr:+ A-B A:CH1 B:CH5

*10-11-26 08:44:04

rig∶SINGLE H1 : OUT ☆ +561.0mV ◇ -561.0mV

RECORDER 10ms ×1/2



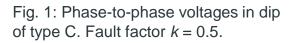


Fig. 2: Phase-to-phase voltages in dip of type D. Fault factor k = 0.5.

500Hz

ch2: 📃 500Hz

 RECORDER
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 csr:+
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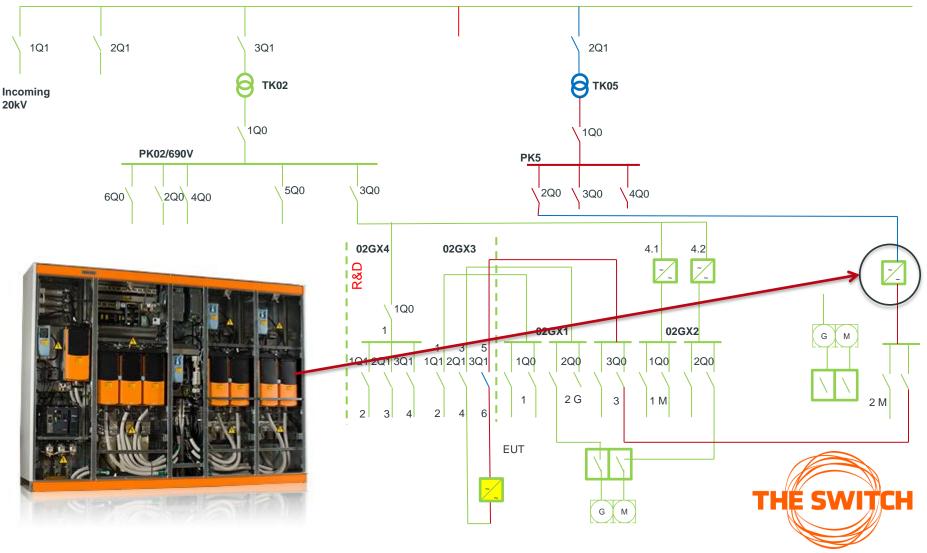
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Fig. 3: Phase-to-phase voltages in dip of type F. Fault factor k = 0.5.



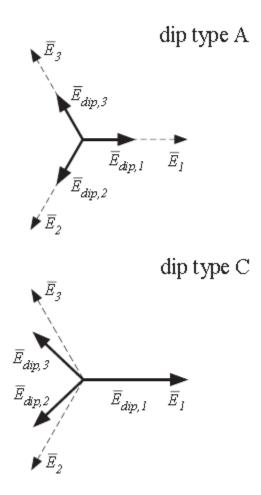
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Full Power Converter Test Facilities



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Some test results with full-scale test bench



Two examples:

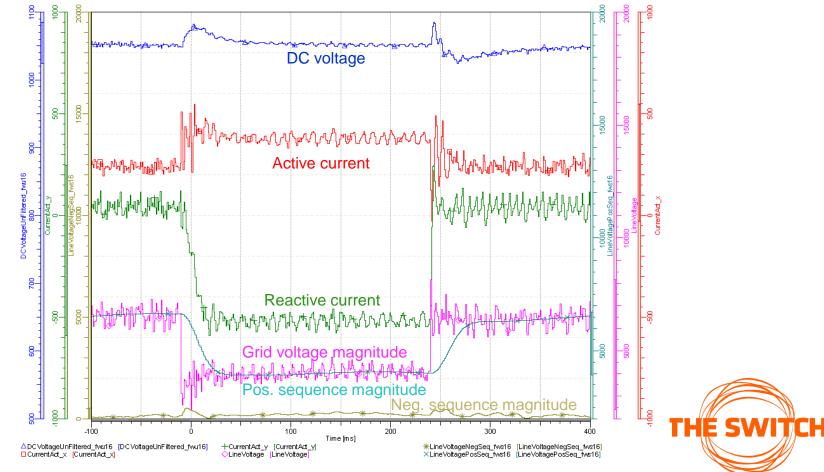
1. 50%/250 ms symmetrical voltage dip (Type A) in 30% load condition

2. 50%⁽¹/250 ms unsymmetric voltage dip (Type C) in 30 % load condition

1) Lowest phase-to-phase voltage is 50% of U_n and corresponds to MV fault factor k = 0.5.

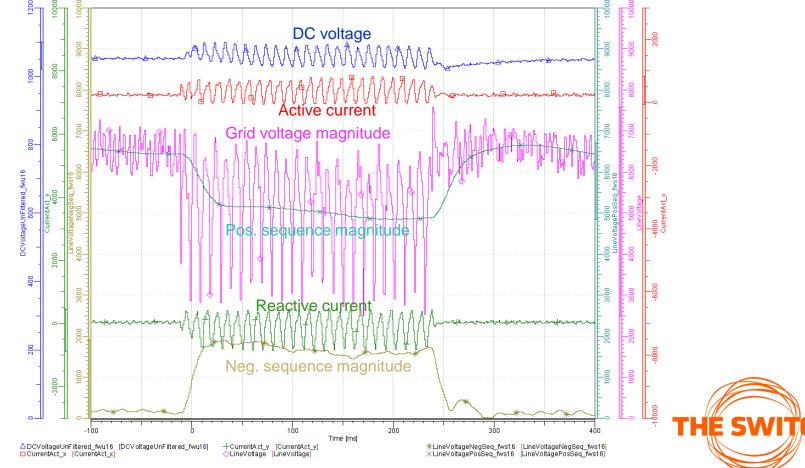
Some test results with full-scale test bench

1. 50%/250 ms symmetrical voltage dip (Type A/A) in 30% load condition



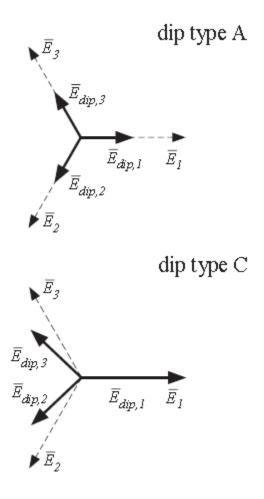
Some test results with full-scale test bench

2. 50%/250 ms unsymmetric voltage dip (Type B/C) in 30 % load condition



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LVRT testing of full power converter



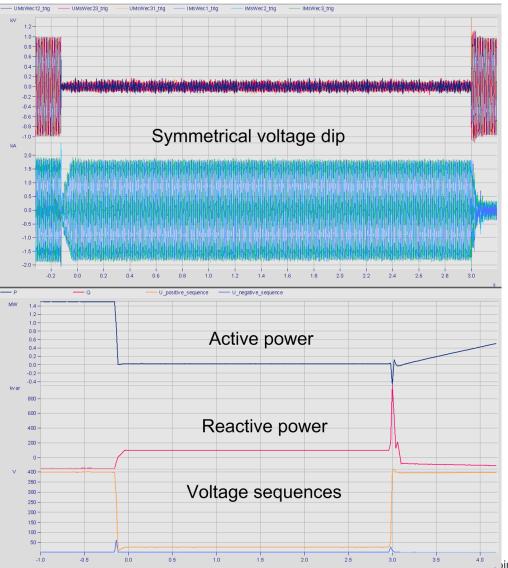
Two examples:

 0% / 3 s symmetrical voltage dip (Type A) in 90% load condition (drive train nominal power is 1.5 MW)

2. 0% / 3 s unsymmetric voltage dip (Type C) in 90 % load condition (drive train nominal power is 1.5 MW)



LVRT testing of full power converter



Key facts

- 1. Symmetrical voltage dip down to 0 % of nominal voltage
- 2. The dip duration was 3 s
- 3. Additional reactive power control was enabled
- 4. Dynamic electrical brake was applied

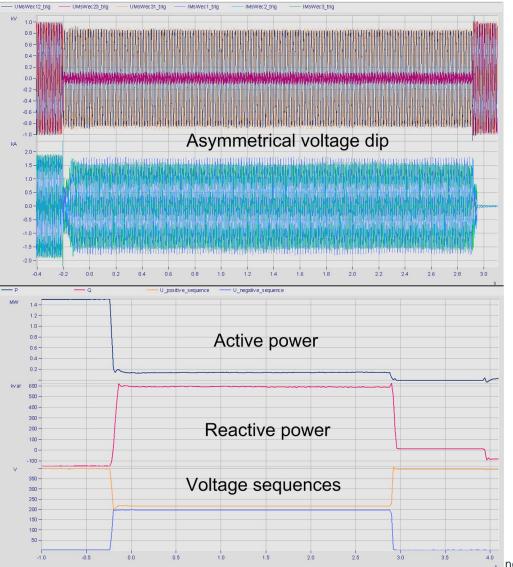


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LVRT testing of full power converter



Key facts

- 1. Asymmetrical voltage dip down to 0 % of nominal voltage
- 2. The dip duration was 3 s
- 3. Additional reactive power control was enabled
- 4. Dynamic electrical brake was used



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Conclusions

- Megawatt-scale full-power converter based test bench for low voltage ride-through testing of wind power converters was proposed
- All types of practical voltage dips occuring on LV-side of Dynconnected WT transformer can be emulated with the test bench
- Arbitrary dip depth (fault factor k), duration and number of consecutive dips can be generated
- Test bench plays a key role in full-power converter product development and product verification
- Could this approach be taken advantage of in certification process of grid code compliance?

Acknowledgements

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